Design of ANFIS Controlled Buck Converter Fed DC Drive Applications

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Abstract

To keep the output of a Buck converter constant despite changes in the input supply, this study develops an ANFIS controller for its regulation. With an emphasis on the design of the ANFIS controller for the control of the Buck converter, this research analyzes the DC/DC converter in order to address the power requirements of a continuous output. In order to regulate the speed of the motor, the resistive load is replaced with a DC motor load, and a speed control loop is introduced. MATLAB/Simulink software is used to conduct the simulation.

1. Introduction

The world's energy crisis is a subject of widespread international worry. It is imperative to identify alternative energy sources because fossil fuels have proven to be both finite and unreliable. When it comes to reliability and availability, renewable energy sources appear to be the best option. Given that renewable energy sources utilize DC-DC converters, there is an increased need for effective DC-DC converters. In situations where a lower voltage is necessary, such as in charger applications, buck converters are used among DC-DC converters. The efficiency of DC-DC converters must be taken into account. The primary purpose of creating these converters is to use them at high frequencies with the least amount of losses, such as switching losses and reverse recovery losses. There have been several ideas put forth for mitigating these losses. The power switches are capable of soft switching thanks to the topology mentioned. Nonetheless, some diodes continue to experience reverse recovery losses, and the complicated auxiliary circuit of this converter results in significant losses that can lower the overall efficiency. A novel resonant circuit-based soft-switched DC-DC buck converter is examined. This architecture employs a resonant circuit made up of a resonant switch, an inductor, a capacitor, and a diode to produce a soft-switching environment for the power switches. The use of a resonant circuit in this arrangement has resulted in the flow of an additional resonant current, which can raise conduction losses. A novel buck converter with zero voltage switching (ZVS) is introduced. In addition to providing soft-switching capability for the switches' turn-on, the use of a tapped inductor and an additional auxiliary circuit also reduces the current flow, allowing for a reduction in conduction losses. Nevertheless, the efficiency is decreased by the reverse recovery losses of the diodes and the turn-off losses of the switches.

In this, ANFIS controller is trained to control the speed of the dc motor using the dc voltage control. The dc voltage control loop for the buck converter is designed with resistive load and speed control loop is added for dc motor load. The data are taken using PI controller based speed control loop and the training of ANFIS control is done using those data.

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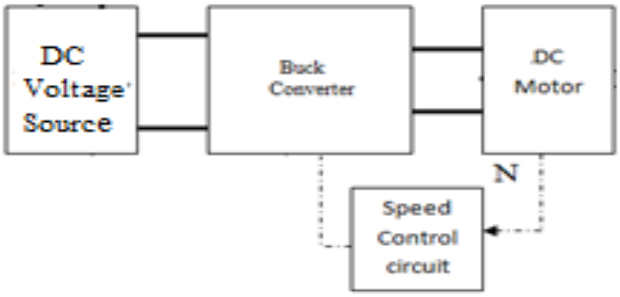
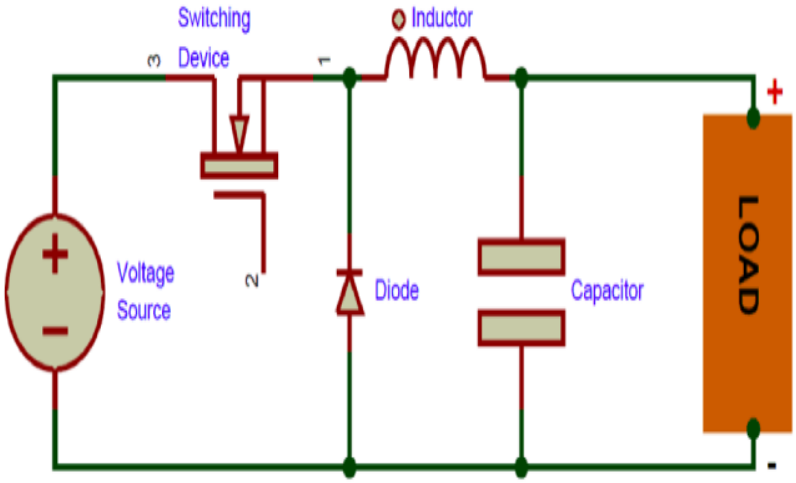
2. Proposed Buck Converter Fed DC Drive

The block diagram is provided below:



The buck converter, which provides power to the dc motor, receives its supply from the dc voltage source in this setup. The motor speed is regulated by the speed control loop with the ANFIS controller by controlling the dc voltage via the buck converter in accordance with the speed requirement.

The buck converter circuit is provided below.



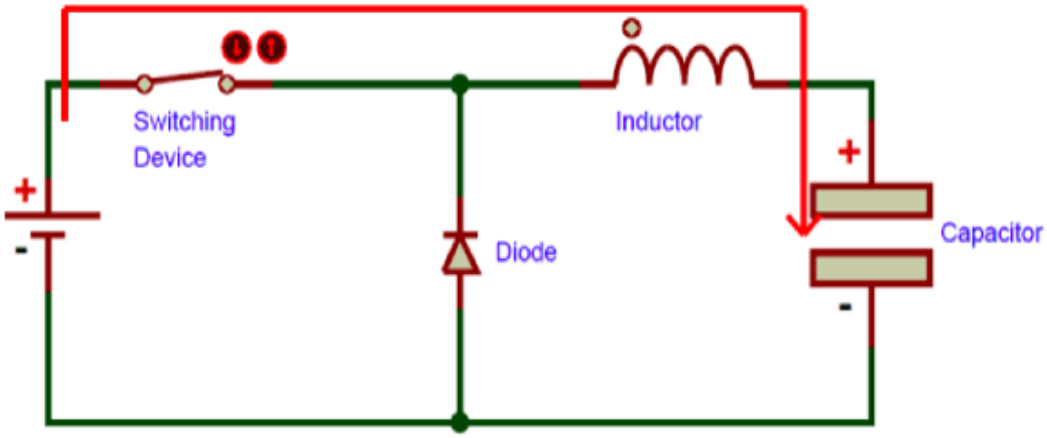
Buck converter circuit

According to the duty ratio of the supplied switching pulse, the buck converter is employed to lower the DC voltage. It consists of a diode, capacitor, switch, and inductor. The load voltage may be less than the input voltage. The following are the buck converter's operational modes:

Mode 1:

The mode1 operational circuit is shown below. At this point, the gate pulse delivered to switch S is HIGH, and the inductor charges throughout this period. The following equations give the inductor voltage and load voltage:

$$V_o = V_{in} - V_L$$



Mode 1Equivalent circuit of buck converter, Vo=Vin-V_L

The diode becomes reverse biased and the inductor current is carried by the switch when the switch is closed (ON) for time period ton. This causes a positive voltage across the inductor.

$$v_{in} = L\frac{di_L}{dt} + v_o$$

Reorganizing the aforementioned equation $$L\frac{di_L}{dt} = v_{in} - v_o$$

The above equation can also be provided as

$$\frac{\Delta i_L}{\Delta t} = \frac{v_{in} - v_o}{L}$$

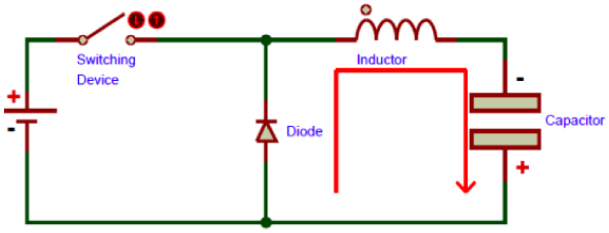
The aforementioned equation is Δt= DT, which is the moment the switch is switched ON. $$\Delta i_{L(closed)} = \left(\frac{v_{in} - v_o}{L}\right) DT$$

where D is the duty ratio.

Mode 2:

The mode2 operational circuit is shown below. The inductor discharges during the time when the gating pulse given for the switch, S, is LOW. The following formula gives the load voltage:

$$V_o = V_L$$



Mode 2Equivalent circuit of buck converter, Vo=V_L

Due to inductive energy storage, the inductor current continues to flow even after the switch is switched off. The current flows via the diode, which is forward-biased, at this time.

$$L\frac{di_L}{dt} = -v_o$$

The aforementioned equation can be written as,

$$\frac{\Delta i_L}{\Delta t} = \frac{-v_o}{L}$$

where is the moment the switch OFF is provided, the above equation is given as

$$\Delta i_{L(open)} = \frac{-v_o}{L}(1 - D)T$$

The total change in inductor current is zero over a single cycle of time period for stable state operation.

$$\Delta i_{L(closed)} + \Delta i_{L(open)} = 0$$

In a steady-state operation, the signal repeats from one cycle to the next, thus the integral function of the inductance voltage VL over a single cycle of time is considered to be zero.

$$\int_0^T v_L\,dt = \int_0^{t_{on}} v_L\,dt + \int_{t_{on}}^T v_L\,dt = 0$$

Where integration over one cycle is defined as T, the time period for one cycle (i. e. , T = ton + toff).

$$(v_{in} - v_o)t_{on} = v_o(T - t_{on})$$

The result of simplifying the aforementioned equation is that

$$D = \frac{v_o}{v_{in}} = \frac{t_{on}}{T}$$

3. Design Procedure For Proposed Converter

1. Ratio of responsibility

The duty ratio is defined as

$$D = \frac{V_o}{V_{in}}$$

The duty cycle is represented by D, the load voltage by Vo, and the source voltage by Vin.

2. Current input

The following equation is used to calculate the source current:

$$I_{in} = \frac{P_{in}}{V_{in}}$$

The source current is at I, the source power at Pin, and the source voltage at Vin.

3. Peak-to-peak amplitude of the inductor current ripple

The inductor ripple current's maximum amplitude is expressed as

$$\Delta I_{l1,l2} = \frac{V_{in} D}{F_S L}$$

With Vin as the input voltage, D as the duty cycle, FS as the converter's switching frequency, and L as the inductance value.

4. Choosing the capacitor and inductor

The inductance value is calculated using the following relation:

$$L \geq \frac{V_{in} D T_S}{2\Delta I_o}$$

Where, TS -Switching cycle and ΔIo load ripple current

The capacitance is calculated using the following relation:

$$C \geq \frac{D V_o}{R \Delta V_o F_S}$$

Where ΔVo –load ripple voltage, R- resistive load, and V o - load voltage.

By modifying the duty cycle of the converter, the PI controller regulates the load voltage. It ensures the buck converter runs smoothly while improving response in both steady state and transient state scenarios.

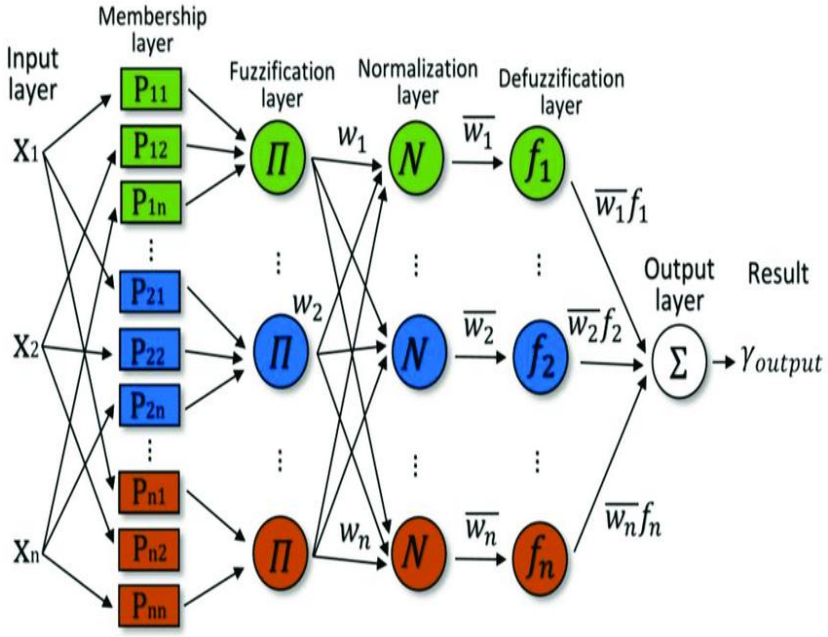
Proposed Control Structure

This converter delivers a regulated dc output voltage even when the load and input voltage fluctuate. The values of the converter's components vary depending on the temperature, pressure, and time. For this reason, the output voltage should be controlled in a closed loop using negative feedback principles. i) Voltage Mode Control .

Through a resistive voltage divider, the output voltage of this control mode converter is controlled and fed back. In a voltage error amplifier, it is compared to a precise external reference voltage, Vref. A control voltage is generated by the error amplifier, which is compared to a constant-amplitude sawtooth waveform. A PWM signal that is sent to the drivers of adjustable switches in the dc-dc converter is produced by either the PWM Modulator or the comparator

Artificial neuro fuzzy inference system

The advantages of both neural networks and fuzzy logic systems are combined in an adaptive neuro fuzzy inference system (ANFIS), a form of artificial intelligence. Like a neural network, ANFIS can learn and make choices using data, but it can also deal with noisy or incomplete data, much like a fuzzy logic system. Because of this, ANFIS is a good fit for applications where the data is always changing or is not always correct.



Architecture diagram of artificial neuro fuzzy inference system

Using ANFIS in AI has several advantages. With its ability to enhance the precision of forecasts produced by AI models, ANFIS is a potent instrument. In addition, using ANFIS can help cut down on the amount of time it takes to train AI models. Additionally, ANFIS is capable of handling the non-linear data that is frequently seen in real-world situations. A neural network used for adaptive learning is called ANFIS. It integrates a learning algorithm with a neuro-fuzzy system. Data can be used by ANFIS to learn and generate predictions. The weights of the connections between the network's neurons may be changed by the learning algorithm. With this, the network may acquire new information and adjust accordingly.

In AI applications, there are several ways to improve ANFIS (Adaptive Neuro-Fuzzy Inference System). Using a more complex neuro-fuzzy system, such as one with a higher-order Takagi-Sugeno fuzzy inference system, is one method. In terms of accuracy and interpretability, this may lead to superior outcomes.

One way to enhance ANFIS is to combine it with other AI approaches, such as evolutionary algorithms. This might help enhance the system and improve its performance. Lastly, it's also crucial to constantly update the ANFIS system with fresh information and data. This may contribute to increasing its accuracy and ensuring that it stays current with the newest developments.

DC–DC Converter Design (100 V to 48 V, 180 W)
Specifications:
Input Voltage = 100 V
Output Voltage = 48 V
Output Power = 180 W
Switching Frequency = 30 kHz

1. Duty Ratio

D = Vo / Vi = 48 / 100 = 0.48

2. Output Current
Io = Po / Vo = 180 / 48 = 3.75 A

3. Inductor Design
Assuming 20% ripple current:
ΔIL = 0.75 A
Equivalent inductance:
Leq = (Vi − Vo)D / (ΔIL fs) ≈ 1.1 mH

Lr = 100 µH (resonant)
Lm = 1mH (magnetizing)

4. Resonant Tank for ZVS
Resonant frequency chosen as twice the switching frequency:
fr = 60 kHz
Cr = 1 / ((2πfr)^2 Lr) ≈ 68 nF

5. Capacitor Design

Assume:

- Voltage ripple ≤ 5% of 48 V
- Ripple voltage ≈ 2.4 V

$$C_1 = C_2 = \frac{I_o D}{\Delta V f_s}$$

Impedance network capacitors:
C1 = C2 = 47 µF

Output capacitor:

Output voltage ripple ≤ 1% of 48 V → 0.48 V

$$C_o = \frac{I_o D}{\Delta V_o f_s}$$

Co = 125 µF

DESIGN of DC MOTOR:

The armature current of the dc motor is given by

$$I_a = \frac{P}{V}$$

Ia = 3.75A.

DC motors typically have 5–15% voltage drop across armature resistance at rated load.

Assume:

- Armature voltage drop ≈ 10% of rated voltage

VRa≈0.1×48=4.8 V

Back EMF:

$$E_b = V - V_{Ra}$$

Eb=43.2V

The armature resistance value is provided below:

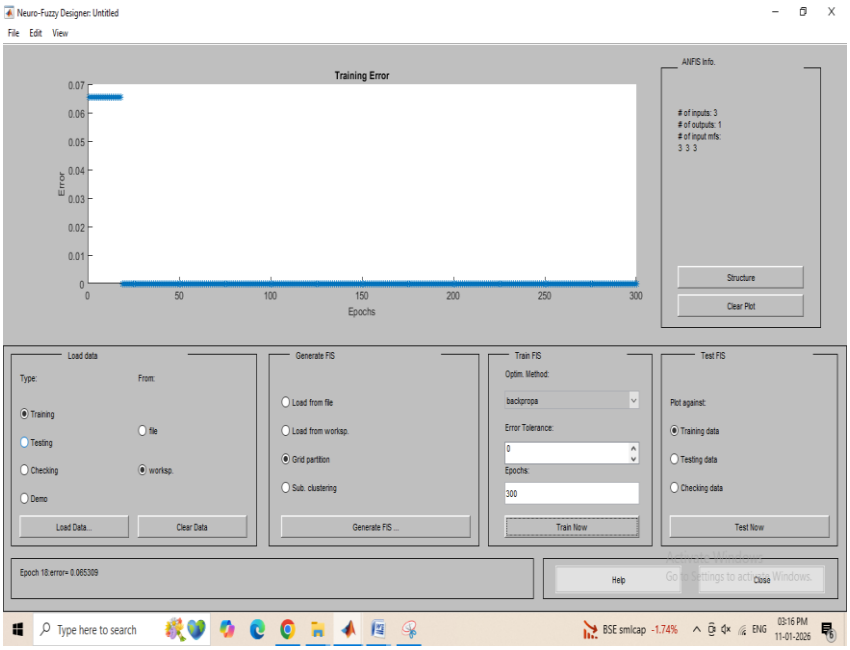
$$R_a = \frac{V - E_b}{I_a}$$

Ra = 1.28Ω**.**

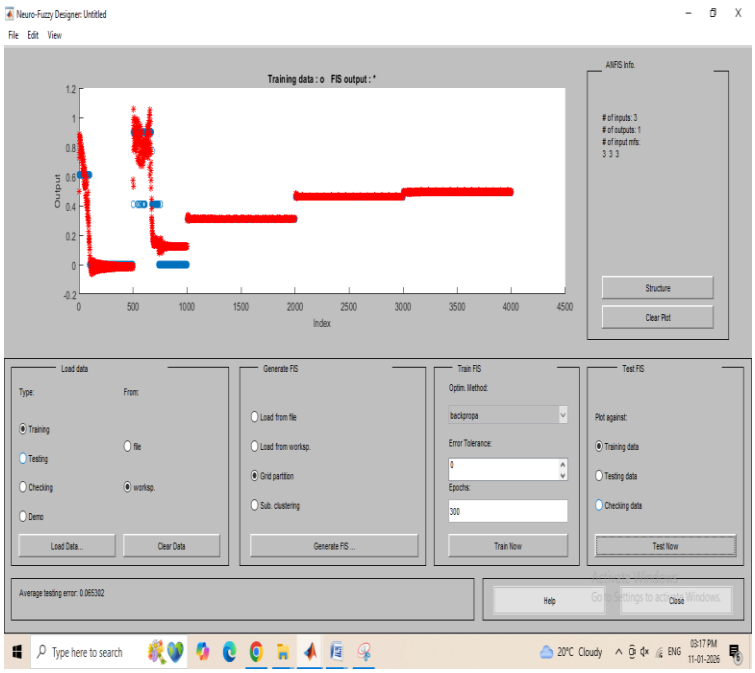
The electrical time constant is provided below:

$$\tau_e = \frac{L_a}{R_a}$$

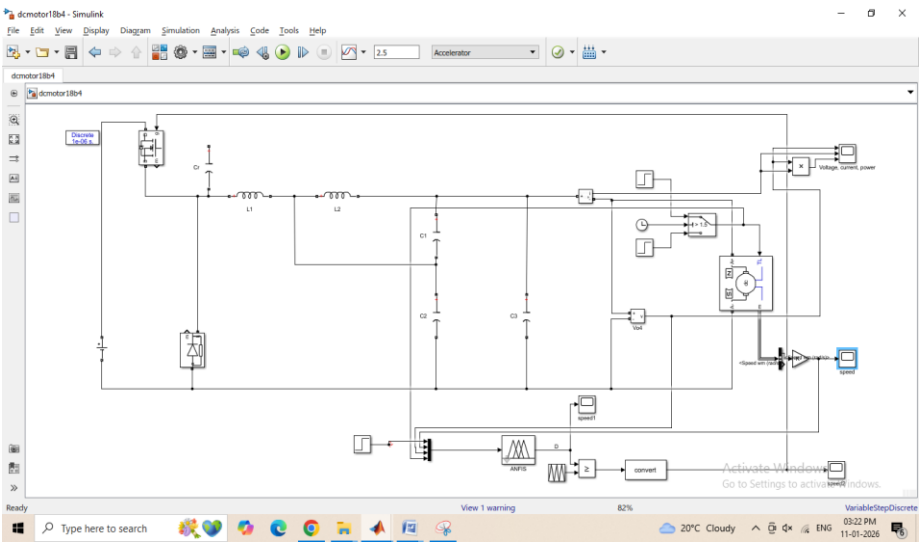
With assuming Te as 5ms, we get La as 6.4 mH.



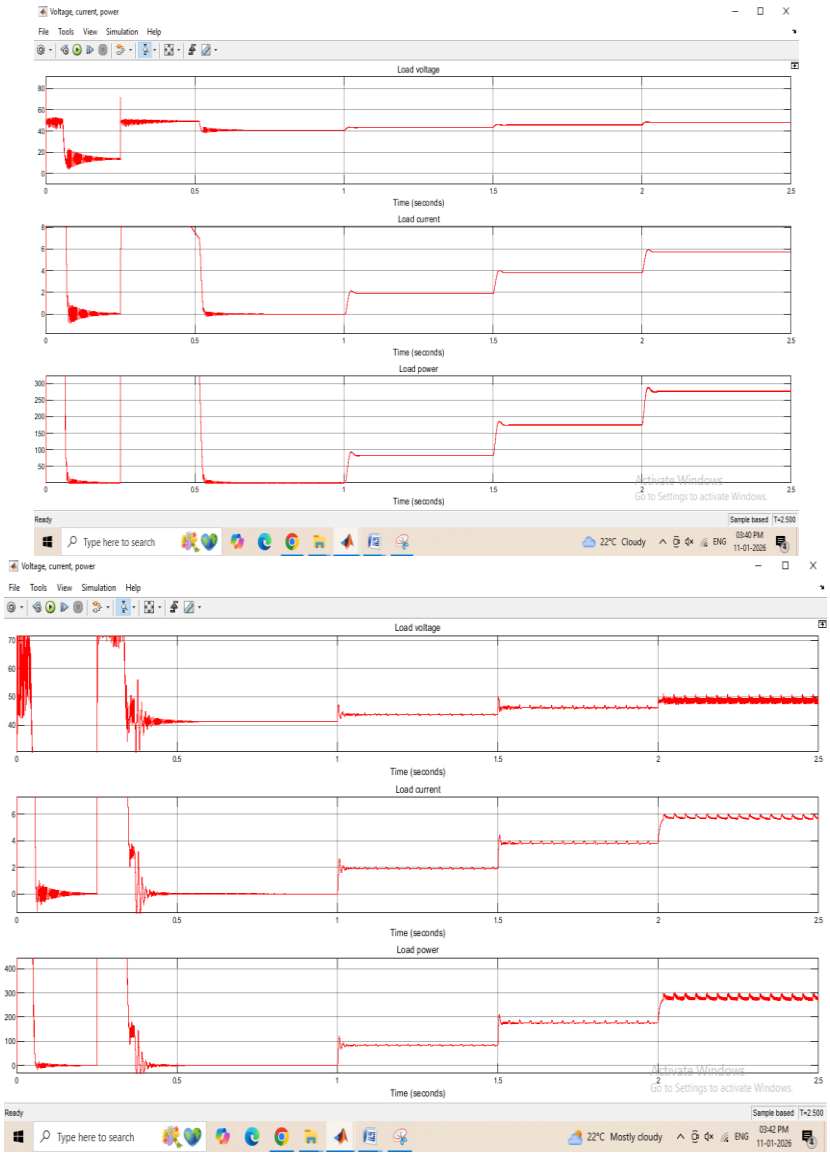
The mean square error is 0.06539. Then the trained controller is tested with the provided data.



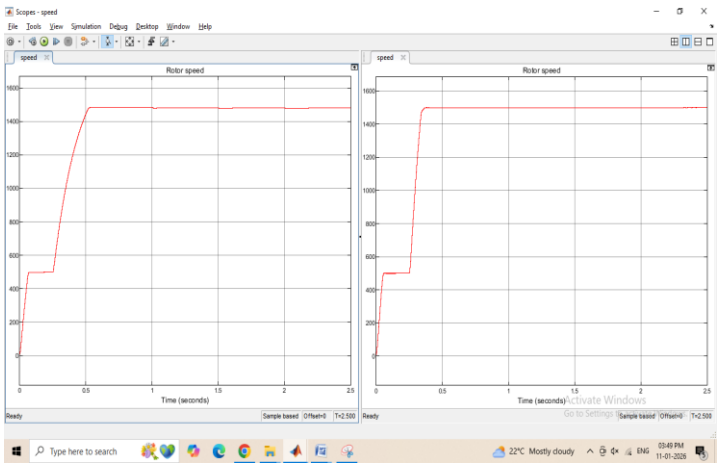
The trained output and tested output is almost similar. Then the controller is saved by exporting to the workspace and then to a separate file. We can access the controller by specifying its name in the fuzzy logic block in the simulation file. The simulation circuit using an ANFIS controller is shown below:



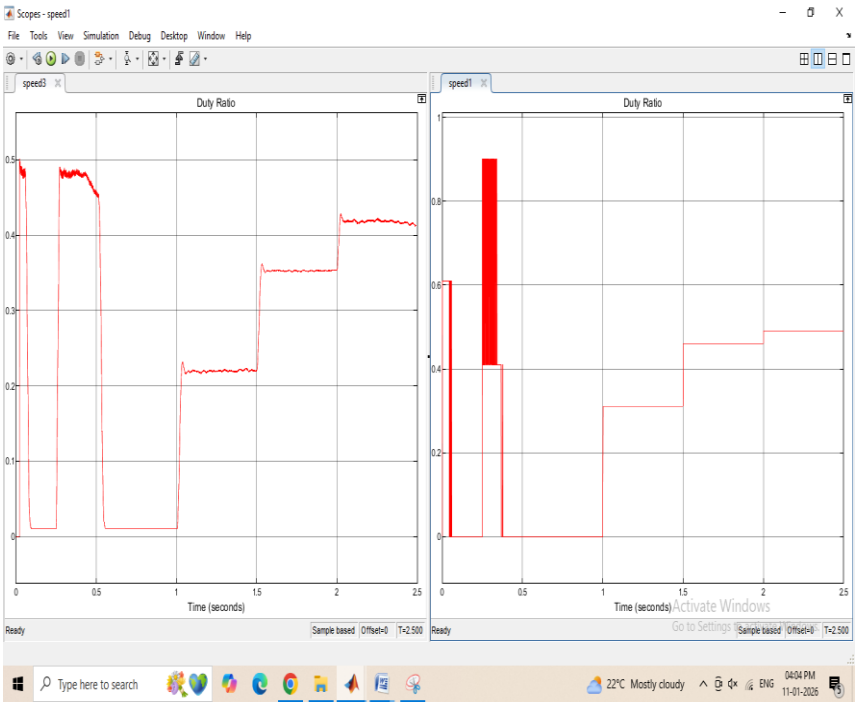
The input voltage is 100V with a load voltage of 48V in this case. At t=0.25 s, the speed reference shifts from 500 rpm to 1500 rpm. The motor starts off operating at NO Load condition with Tm=0, then at t=1s the torque is delivered as 0.5Nm, at t=1.5s as 1Nm, and at t=2s as 1.5Nm (overloading). The voltage current and power of the dc motor load at various conditions with PI and ANFIS is provided below:



In this, the voltage is around 48V and current is around 4A with power of 180W in full load condition (Tm=1Nm) and the power consumption is around 280W during overloaded conditions (Tm=1.5Nm). The speed of the dc motor with PI controller and ANFIS controller is provided below:



With PI controller, the speed is settled at 500 rpm at no load condition (Tm=0) is around is 0.07s with rise time 0.06s and steady state error is 1.5 rpm and with reference speed as 1500 rpm, settling time is around is 0.06s with rise time 0.05s and steady state error is 0.3 rpm. The duty ratio variations of the PI controller and ANFIS controller is provided below:



With PI controller the duty ratio variations is around from 0.01 to 0.48 and with ANFIS the duty ratio varies from 0 to 0.8. The comparison of the performance of PI controller and ANFIS controller is provided below:

Parameters	**Nr=500rpm**		**Nr=1500 rpm**							
	Tm=0Nm		**Tm=0Nm**		**Tm =0.5Nm**		**Tm=1Nm**		**Tm=1.5Nm**	
	PI	**ANFIS**	**PI**	**ANFIS**	**PI**	**ANFIS**	**PI**	**ANFIS**	**PI**	**ANFIS**
Rise time(s)	0.06	**0.05**	0.271	**0.1**	0.04	**0.005**	0.03	**0.005**	0.03	**0.025**
Settling time(s)	0.07	**0.06**	0.29	**0.15**	0.24	**0.025**	0.32	**0.015**	0.41	**0.25**
Steady state error (rpm)	1.5	**0.3**	17.1	**0.35**	18.6	**0.85**	19	**1.05**	19.4	**0.3**

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